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| **Course Name:** | **Basic Electronic Circuits** | **Semester:** | **III** |
| **Date of Performance:** | **28/9** | **Batch No:** | **B2** |
| **Faculty Name:** | **BPK** | **Roll No:** | **1912052** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **/25** |

**Experiment No: 6**

**Title: Study of BJT Biasing**

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| **Aim and Objective of the Experiment:** Study of BJT Biasing |
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| **COs to be achieved:** |
| **CO2**. |

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| **Theory:** |
| Transistor Biasing:  For the proper functioning of transistor we would want that the Q-point should be at the center of the load line. But, there is vacation in Q-point because, collector current (Ic) is a function of temperature, device parameters, and base to emitter voltage (Vbe). The process of stabilizing collector current (Ic) against all the above variations is called as transistor biasing.  Stability:  The stability of Q-point is dependent on reverse saturation current (Icbo),Base-emitter  voltage (Vbe),and Current amplification factor (βdc).  Therefore, we have three stability factors as follows:  1. S = Δ Ic / Δ Icbo (when Vbe and βdc are constant.)  2. S’ = Δ Ic / Δ Vbe (When Icbo and βdc are constant.)  3. S’’ = Δ Ic / Δ βdc (when Vbe and Icbo are constant.)  Types of biasing:  Fixed bias without Re. In this method, a high resistance RB is connected between base and Vcc. The stability factors for this circuit are: S = Δ Ic / Δ Icbo = 1+ βdc. S’ = Δ Ic / Δ Vbe = - βdc/Rb. S’’ = Δ Ic / Δ βdc = Ic / βdc. Advantages: 1. The fixed bias circuit is simple and has less no. of components. 2. It gives very good flexibility as the Q-point can be selected at any point in the active region by adjusting the value by Rb. Disadvantages: 1. Very poor thermal stability as, S= 1+ βdc. 2.  As all the stability factors depend on βdc, any small change in βdc will shift the position of Q-point.  Fixed bias with RE.  In the circuit only a resistor Re is added to the fixed bias ckt. The advantage of adding Re in the circuit is that it stabilizes collector current (Ic) temp and βdc. Now if the collector current tends to increase due to either rise in temp. or due to change in βdc, due to transistor replacement, than the emitter current (Ie) will also increase or , thus the voltage drop across Re will also increase, resulting in reduction of base current. This decrease in base current will decrease collector current, and hence the collector current will be stabilized. The stability factor for fixed bias circuit is given as: S = Δ Ic / Δ Icbo = 1+ βdc./(1+ βdc(Re/(Rb+Re))) S’ = Δ Ic / Δ Vbe = - βdc/(Rb+(1+ βdc)Re). S’’ = Δ Ic / Δ βdc = Ic / βdc.  • Collector bias. In this circuit to improve the level of stability a feedback path is introduced from collector to base. The feedback used is negative feedback and hence it helps in stabilization of Qpoint. The stability factors for this circuit. Are as follows: S = Δ Ic / Δ Icbo = (1+ βdc.)/(1+ βdc(Rc/(Rc+Rb))) S’ = Δ Ic / Δ Vbe = - βdc/( βdc Rc+Rc+Rb). S’’ = Δ Ic / Δ βdc = Ic(Rc+Rb) / (βdc(Rb+Rc(1+ βdc)))  • Voltage divider bias. Resistors R1 & R2 provide biasing and RE provides stabilization of Q-point. In this change in Collector current (Ic) with respect to change in reverse saturation current depends on the ratio of Rth /RE. If Rth/RE is very less, than the value of S=1.The stability factor for this circuit is as follows; S =ΔIc/Δ Icbo = (1+ βdc.)(1+(Rth/RE)/(1+ βdc+(Rth/RE)) S’ = Δ Ic / Δ Vbe = - βdc/( βdc RE+RE+RB). S’’ = Δ Ic / Δ βdc = Ic S / (βdc (1+ βdc)). |

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| **Circuit Diagram/ Block Diagram:** |
| **Fixed bias circuit**      **Collector to base bias circuit**      **Potential divider bias** |
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| **Stepwise-Procedure:** |
| 1. Open a new Schematic. 2. Draw the Circuit As Shown. 3. Note down the parameters as per the observation table. |

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| **Observation Table:**   |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Biasing circuits | Ic(Q) | | IB(Q) | | VBE (Q) | | VCE(Q) | | | Obs. | Cal. | Obs. | Cal. | Obs. | Cal. | Obs. | Cal. | | Fixed bias | 0.00995112 | 0.001 | 0.00092653 | 0.00093 | 9.265299 | 9.2 | -0.6858183 | -276 | | Collector to base bias | 0.00879046 | 0.0088 | 4.50323e-05 | 4.4e-05 | 9.285811 | 9.2 | 0.450321 | 1.1 | | Voltage divider bias | 0.00390947 | 0.0059 | 1.88822e-05 | 2.9e-05 | 9.410747 | 9.2 | 5.501277 | -5.8 | |
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| **Calculation:** |
| 1. Q-point values of all the biasing circuits.  2. Stability factor S for all the biasing circuits. |

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| **Waveform** |
| No waveforms |

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| **Post Lab Subjective/Objective type Questions: (hand written)** |
| 1. In the circuit shown below, β =100 and VBE=0.7V. The Zener diode has a breakdown voltage of 6V. Find the operating point. [electronic-devices-circuits-questions-answers-collector-base-bias-q9](https://www.sanfoundry.com/wp-content/uploads/2018/02/electronic-devices-circuits-questions-answers-collector-base-bias-q9.png)  2. The collector current (IC) that is obtained in a collector to base biased transistor is\_\_\_\_\_\_\_\_\_ 3.The collector to emitter voltage (VCE) is obtained by\_\_\_\_\_\_\_\_\_  4. What is the DC characteristic used to prove that the transistor is indeed biased in saturation mode? |

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| **Conclusion: (to be written in own words)** |
| We learned about Fixed biasing potential divider biasing and base to collector biasing. |

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| **Signature of faculty in-charge with Date:** |